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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,569	08/30/2000	Joseph E. Geusic	303.390US3	9738

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EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/650,569	GEUSIC ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *39-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39,41-46,48,50-53,55,57-60,62,64,65,68,70 and 71* is/are rejected.

7)☒ Claim(s) *40,47,49,54,56,61,63,67,69 and 72* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The rejections to claims 39-46, 48-53, 55-60 and 62-71 under double patenting as set in paper No. 6 are withdrawn in response to applicants' amendment.

Specification

2. The abstract of the disclosure is objected to because the patent number of the parent of this case is missing. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

3. Claims 39, 42, 48 and 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanber (U.S. 5,312,765) in view of Chino (U.S. 5,796,714).

In reference to claim 1, Kanber (Fig.1-10) teaches an analogous method to form an electronic system including a first functional circuit (16) interconnected to a second functional circuit (24) interconnect comprising forming the first functional circuit (16) on a first surface (12) of a semiconductor substrate (10); forming a second functional circuit (24) on a second surface (14) of the semiconductor surface; forming hollow vias (92) suitable for optical signal (column 6, lines 9-17); and interconnecting the first (12) and second (24) functional circuits together by the hollow vias (92) (column 2, line 64 – column 6, line 44).

Kanber do not teach the steps of forming an optical fiber having a cladding layer and a core in the hole. However, Chino et al. teach an analogous method to form integrated circuits including the steps of forming a hole (121) in a substrate (12) having a cladding layer (125) and a hole (125) in the hole (121) suitable for interconnections (column 12, lines 36-60).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the hole in the substrate having a cladding layer and a core as taught by Chino et al. into the electronic system of Kanber since the incorporation of optical fibers having a cladding layer and a core in a hole provide optimum emission characteristics by eliminating the signal degradation (column 1, lines 42-52 and column 4, lines 18-24).

In reference to claims 42 and 51, Chino teaches that the formation of the optical fiber comprises forming a core with a core hole, the core hole substantially along the center of the optical fiber (column 12, lines 36-60).

4. Claims 41, 43, 44 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanber ('765) and Chino et al. ('714) as applied to claim 39, 42, 48 and 51 above, and further in view of Gaul (U.S. 5,618,752).

In reference to claim 41, 43, 44 and 50 Kanber in combination with Chino et al. teaches that the cladding layer surrounds the core but fails to expressly teach that the cladding layer and that the core has different indexes of refraction. However, Gaul (Fig. 2A) teaches an analogous method to form interconnections through semiconductor substrates including a cladding layer (216) made of a wall oxide and a core (217) made of doped polysilicon. As to claim 43 Gaul teaches using the same material as that of the claimed invention. Therefore, it is clear that the refractive indexes are the same.

It would have been obvious to include a core and a cladding layer with different refraction indexes as taught by Gaul into the combination of Kanber and Chino et al. since the addition of the core would provide a connection to mountable circuit boards

(column 2, lines 33-39), meanwhile surrounding the polysilicon with an oxide layer having a different refractive index would prevent noise from degrading the signal (column 2, lines 53-65).

5. Claims 45-46 and 52-53, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanber ('765) in view of Chino et al. ('714) as applied to claims 39, 42, 48 and 51 above, and further in view of Gaul ('752) and Suzuki (U.S. 5,362,976).

In reference to claims 45-46 and 52-53 Kanber in combination with Chino et al. teaches all aspects of the invention but fails to teach that the first and second functional circuits together includes coupling a node of the first functional circuit to a first end of the optical fiber and coupling a node of the second functional circuit to a second end of the optical fiber, said nodes are coupled using an optical transmitter and an optical receiver. However, Gaul teaches (Fig.5) two substrates (341 and 343) optically connected through a fiber optic material aligned with an optical transmitter (346) and an optical receiver (345) (column 11, lines 36-60).

Therefore, it would have been obvious to one skilled in the art at the time of the invention was made to include the optical connection as taught by Gaul into the electronic system of Kanber and Chino et al. since the addition fiber optic materials along with metal interconnections allows the integration of different circuitry within the system (column 3, lines 3-7).

Kanber in combination with Chino et al. and Gaul do not show that the first and second nodes are coupled together with the ends of the optical fiber. However Suzuki shows a semiconductor device having an optical package including coupling a node on

a semiconductor device chip to a first end of the optical fiber (9) to and coupling a node a circuit substrate to a second end of the optical fiber (column 2, lines 3-23).

Therefore, it would have been obvious to one skilled in the art at the time of the invention was made to incorporate the optical package of Suzuki into the electronic system of Kanber, Chino et al. and Gaul since packaging semiconductor substrates and interconnecting them with fiber optics allows the narrowing of interconnections within said substrates without increasing parasitic capacitance between metal patterned conductors (column 1, lines 50-60)

6. Claims 55, 57-58, 62 and 67-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaul ('752) in view of Chino et al. ('714) and Kanber ('765).

In reference to claims 55, 62 and 68, Gaul in the first embodiment of the invention (Fig.1A-1I) teaches forming an electronic system including the steps of forming a first functional circuit (214) on a first surface (112) of a first semiconductor substrate (111); forming a hole (130) through the first semiconductor substrate; and bonding the first (111) and second substrate (116) together (column 4, line 48 – column 7, line 29). Also, Gaul in another embodiment of the invention (Fig.2A-2D) teaches forming a second functional circuit (222) after forming the first functional circuit (214), and forming a cladding layer and a core which are made of the same material as of the claimed invention. Gaul further teaches forming a hole in the first substrate followed by forming a second hole on the second substrate and bonding them such that first hole and the second hole are in alignment (Fig.4P).

Gaul does not expressly teach forming an optical fiber having a cladding layer and a core in the hole. Nevertheless, Chino et al. teach an analogous method to form integrated circuits including the steps of forming a hole (121) in a substrate (12) having a cladding layer (125) and a hole (125) in the hole (121) suitable for interconnections (column 12, lines 36-60).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the hole in the substrate having a cladding layer and a core as taught by Chino et al. into the electronic system of Gaul since the incorporation of optical fibers having clad layer and cores in a hole provide optimum emission characteristics by eliminating the signal degradation (column 1, lines 42-52 and column 4, lines 18-24).

Gaul in view of Chino et al. does not teach interconnecting the first and second functional circuit together via the optical fiber. However, Kanber teaches an analogous method forming hollow vias (92) suitable for optical signal (column 6, lines 9-17); and interconnecting the first (12) and second (24) functional circuits together by the hollow vias (92) (column 2, line 64 – column 6, line 44).

Therefore, it would have been obvious to one skilled in the art at the time of the invention was made to include the optical interconnects of Kamber into the electronic system of Gaul and Chino et al. since the combination of various device technologies allows a greater integration of integrated circuits, reducing the damage rate through the manufacturing of the integrated circuit and strengthen the wafer (column 1, line 17 – column 2, line 2).

In reference to claim 57, Gaul (Fig. 2A) in an analogous method to form interconnections through semiconductor substrates teaches including a cladding layer (216) made of a wall oxide and a core (217) made of doped polysilicon. Since Gaul teaches using the same materials as that of the claimed invention, it is clear that the refractive indexes are the same.

In reference to claim 58 Chino et al. teaches that the optical fiber comprises forming a core with a core hole, the core hole running substantially along the center of the optical fiber (column 12, lines 36-60).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate core having a core hole as taught by Chino et al. into the electronic system of Gaul since the incorporation of optical fibers having clad layer and cores in a hole provide optimum emission characteristics by eliminating the signal degradation (column 1, lines 42-52 and column 4, lines 18-24).

7. Claims 59-60, 64-65 and 70-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaul ('752) in view of Kanber ('765) and Chino et al. ('714) as applied to claims 55, 57-58, 62 and 67-68 above, and further in view of Suzuki ('976).

In reference to claims 59-60, 64-65 and 70-71, Gaul in combination with Kanber and Chino et al. teaches (Fig.5) two substrates (341 and 343) optically connected through a fiber optic material aligned with an optical transmitter (346) and an optical receiver (345).

Gaul in combination with Kanber and Chino et al. do not show that the first and second nodes are coupled together with the ends of the optical fiber. However, Suzuki

shows a semiconductor device having an optical package including coupling a node on a semiconductor device chip to a first end of the optical fiber (9) to and coupling a node a circuit substrate to a second end of the optical fiber (column 2, lines 3-23).

Therefore, it would have been obvious to one skilled in the art at the time of the invention was made to incorporate the optical package of Suzuki into the electrical system of Gaul, Kanber and Chino since packaging semiconductor substrates and interconnecting them with fiber optics allows the narrowing of interconnections within said substrates without increasing parasitic capacitance between metal patterned conductors (column 1, lines 50-60)

Allowable Subject Matter

1. Claims 40, 47, 49, 54, 56, 61, 63, 66-67, 69 and 72 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

2. The following is a statement of reasons for the indication of allowable subject matter:

In reference to claims 40, 47, 49, 54, 56, 63, 66, 69 and 72, the prior art of record, Gaul to '752 (Fig.1B) teaches forming an etch pit at a selected location of the first surface of the semiconductor surface; and forming a fiber optic material in alignment with an optical transmitter and an optical receiver

However, Gaul fails to teach or suggest forming the hole by performing an anode etch of the semiconductor substrate such that the hole is formed at the location of the pit; nor that lining said hole with a reflecting mirror prior to forming the cladding layer.

Conclusion

3. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432** . The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

Wael Fahmy

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